EGC442
Class Notes
1/27/2023

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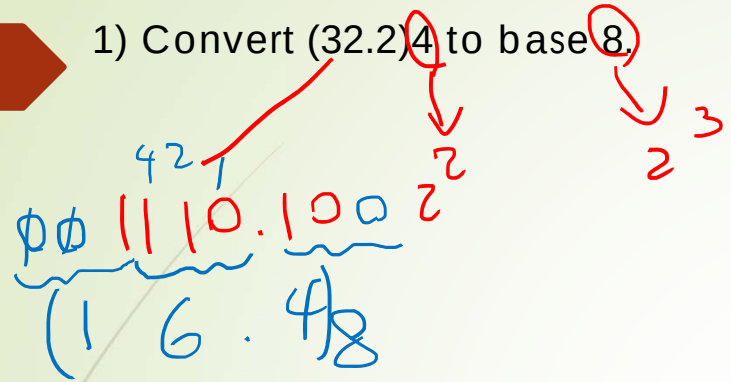
1) Convert (32.2)4 to base 8.



2) Convert (1E2.C1)16 directly base 2.

8421

3/ C.

$(35)_{10}$

$\times (52)_7$

$10 \div 7 = 1$ R = 3

$7 \div 7 = 1$ R = 0

$25 \div 7 = 3$ R = 4

$18 \div 7 = 2$ R = 4

$$\begin{array}{r} 103 \\ +\ 244 \\ \hline (254.3)_7 \end{array}$$

5) Using a total of 8 bits, represent -123 in signed 2's complement format.

+123

−123

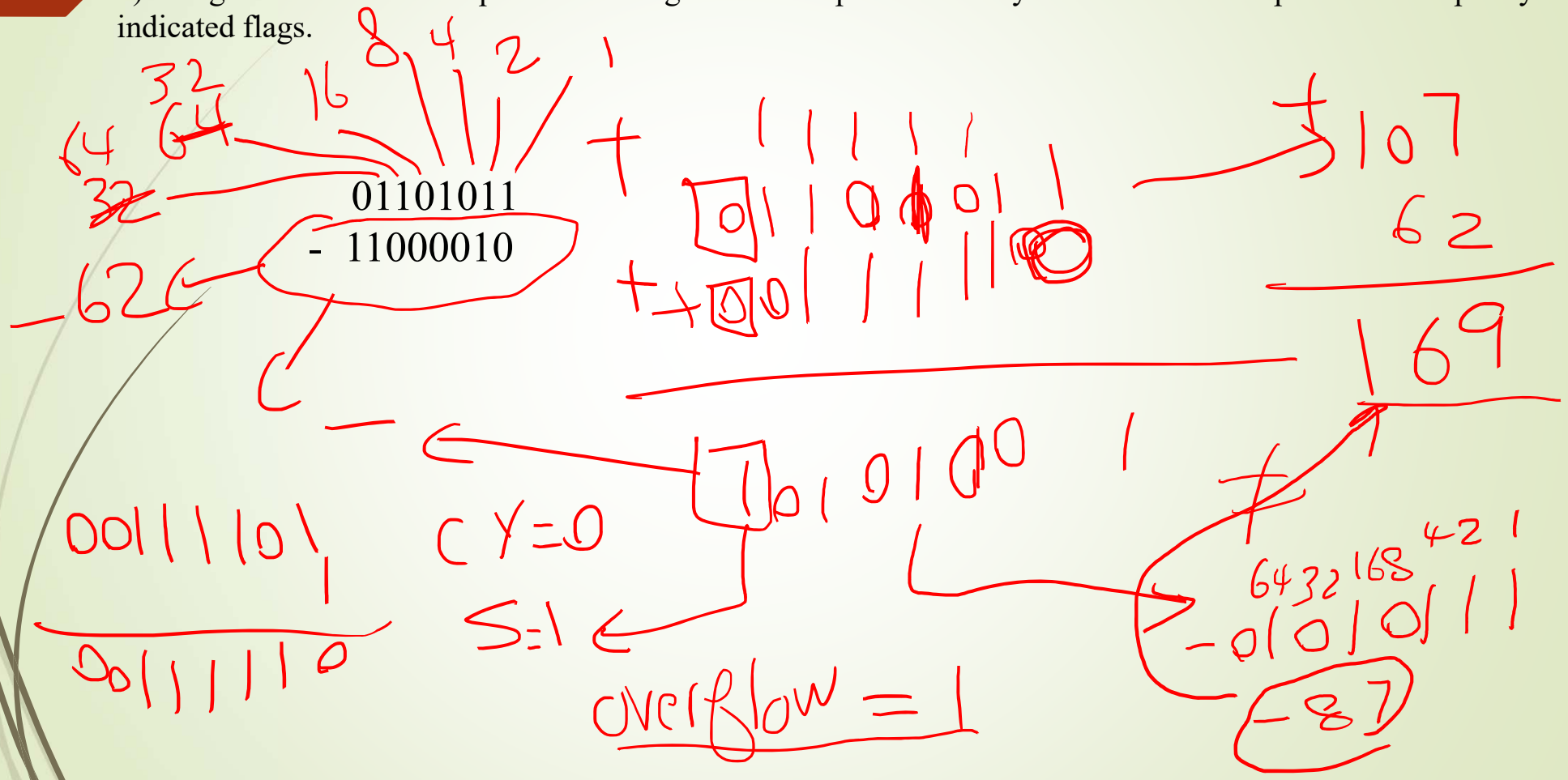
S 64 32 16 8 4 2 1

x x x x x x x x

0 1 1 1 1 0 1 1

1 0 0 0 0 1 0 1

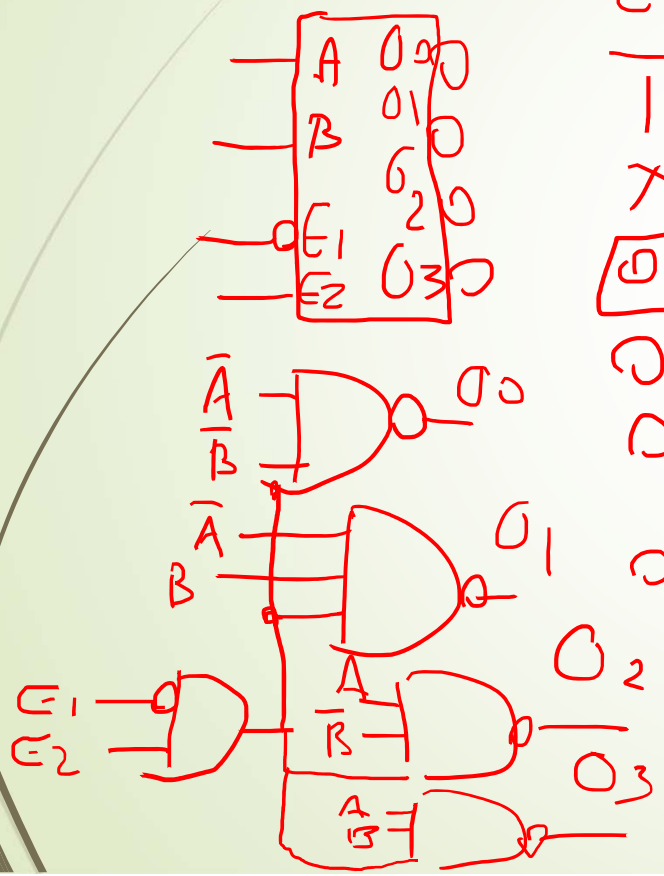
6) The given numbers are represented in signed 2's complement. Carry out the indicated operation and specify the indicated flags.



10) Show the **truth table only** of a combinational circuit that multiplies two numbers A (A_1A_0) and B (B_1B_0). The range of A is 0 to 2 and the range of B is 1 to 3.

A_1	A_0	B_1	B_0	M_2	M_1	M_0
X	X	0	0	X	X	X
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	1
1	0	0	1	0	1	0
1	0	1	0	1	0	0 → 4
1	0	1	1	1	1	0 → 6
1	1	X	X	X	X	X

11) Design a 1-out-of-4 decoder with low active outputs and two enable lines, one active high and the other active low. Show the block diagram, the truth table and the internal circuitry.



E_1	$\bar{E}_2$	A	B	O_3	O_2	O_1	O_0
1	X	X	X	1	1	1	1
X	0	X	X	1	1	1	1
0	1	0	0	1	1	1	0
0	1	0	1	1	1	0	1
0	1	1	0	1	0	1	1
0	1	1	1	0	1	1	1

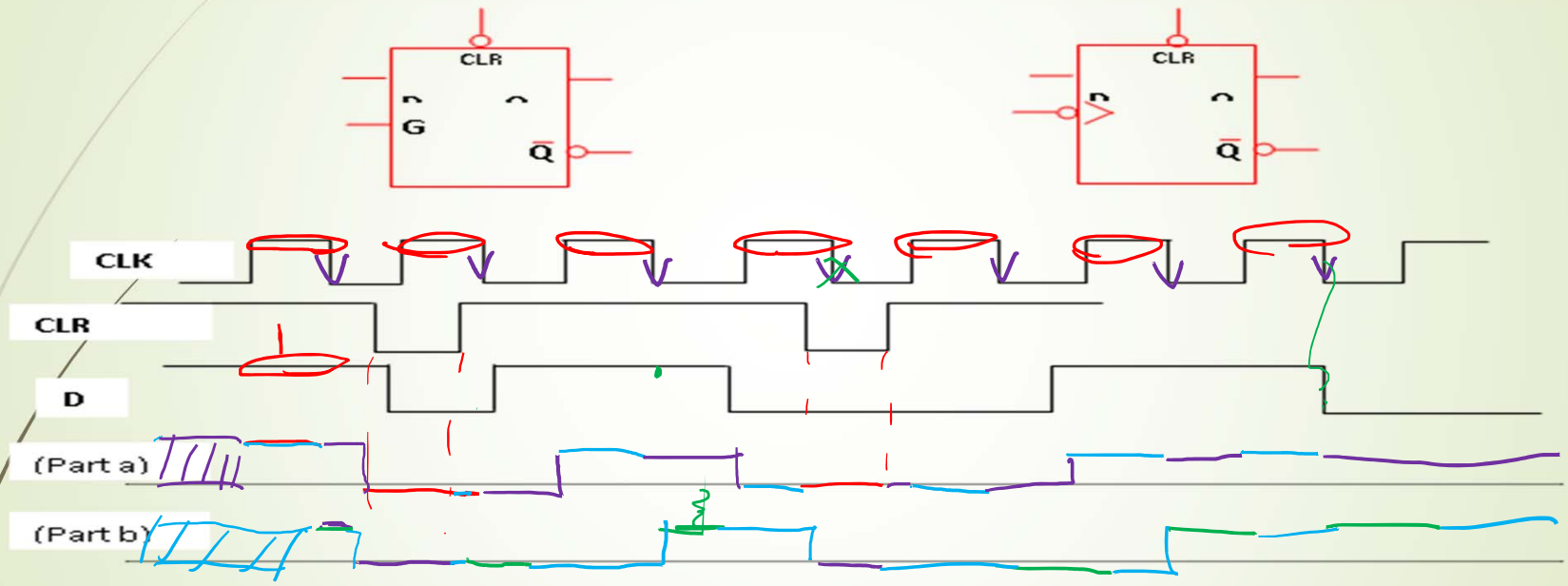
$\bar{O}_0 = \bar{E}_1 \bar{E}_2 \bar{A} \bar{B}$

$\bar{O}_1 = \bar{E}_1 \bar{E}_2 \bar{A} B$

$\bar{O}_2 = \bar{E}_1 \bar{E}_2 A \bar{B}$

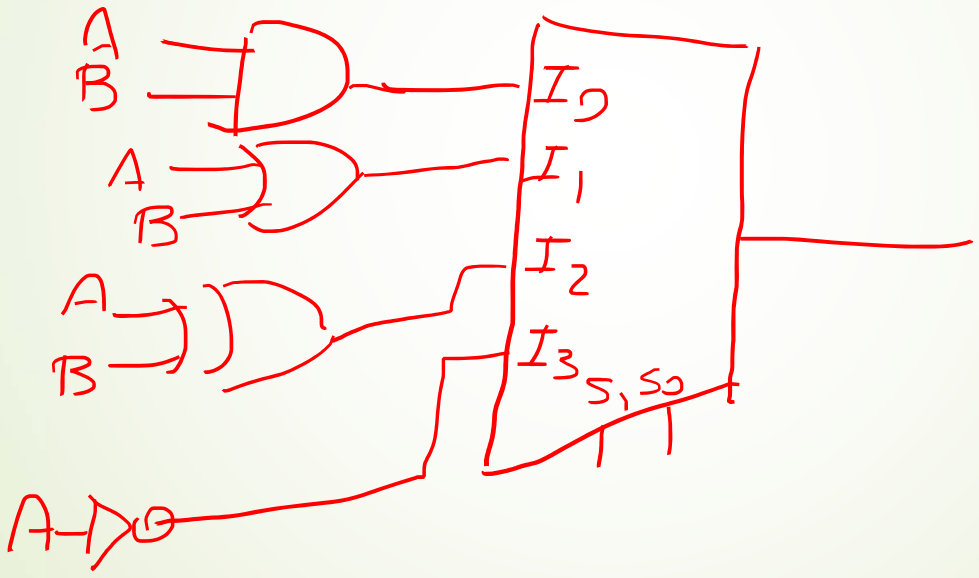
$\bar{O}_3 = \bar{E}_1 \bar{E}_2 A B$

16) Complete the following timing diagram for the given device. Assume Q to be initially 0.



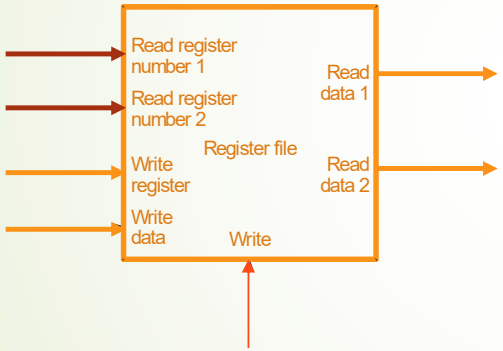
15) Using gates and multiplexer(s), design a one-bit ALU that performs the following logical op

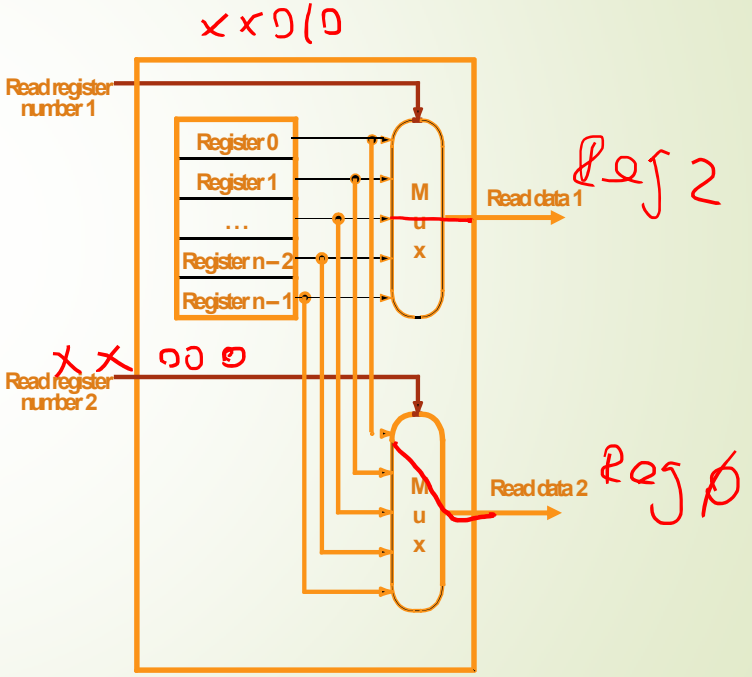
S_1	S_0	Function
0	0	AND
0	1	OR
1	0	XOR
1	1	NOT



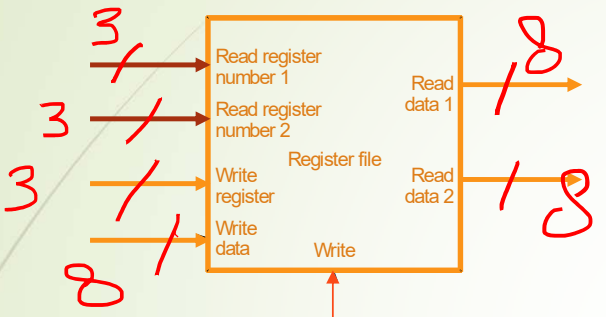
Design of Processor's Register File

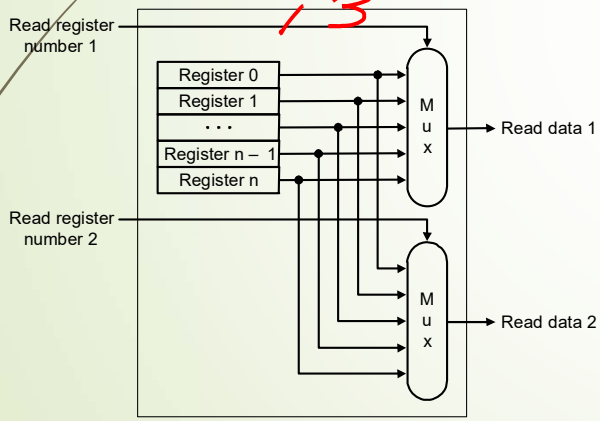
- Ability to read from two registers and write to one register
- Read operation using D flip-flops and MUX's

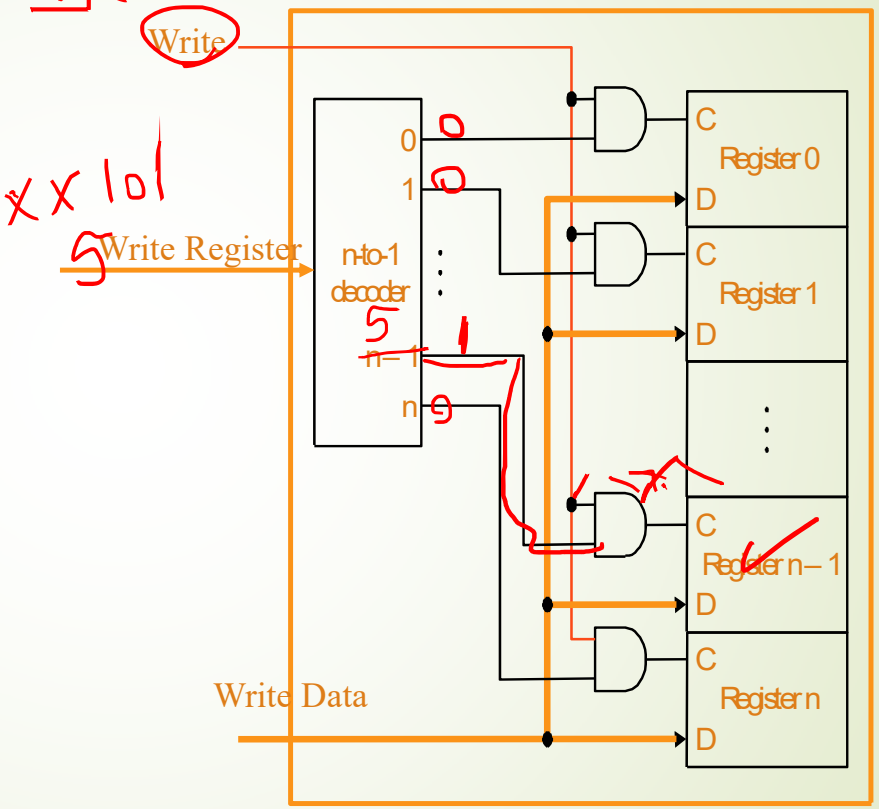




Register File – Read and Write



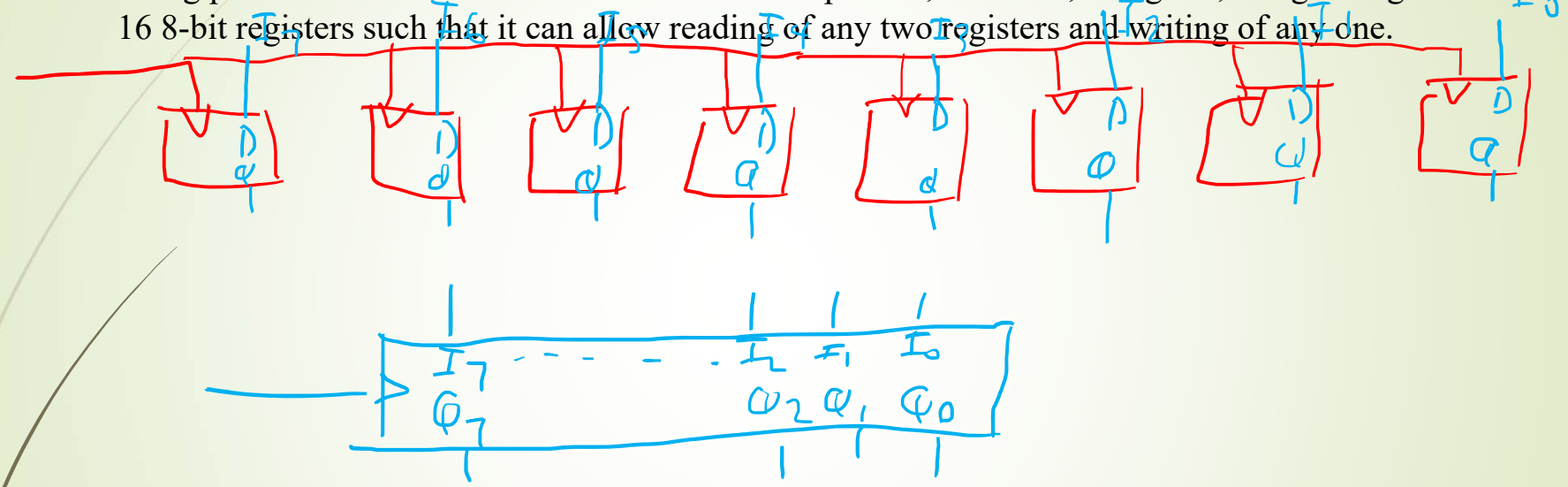


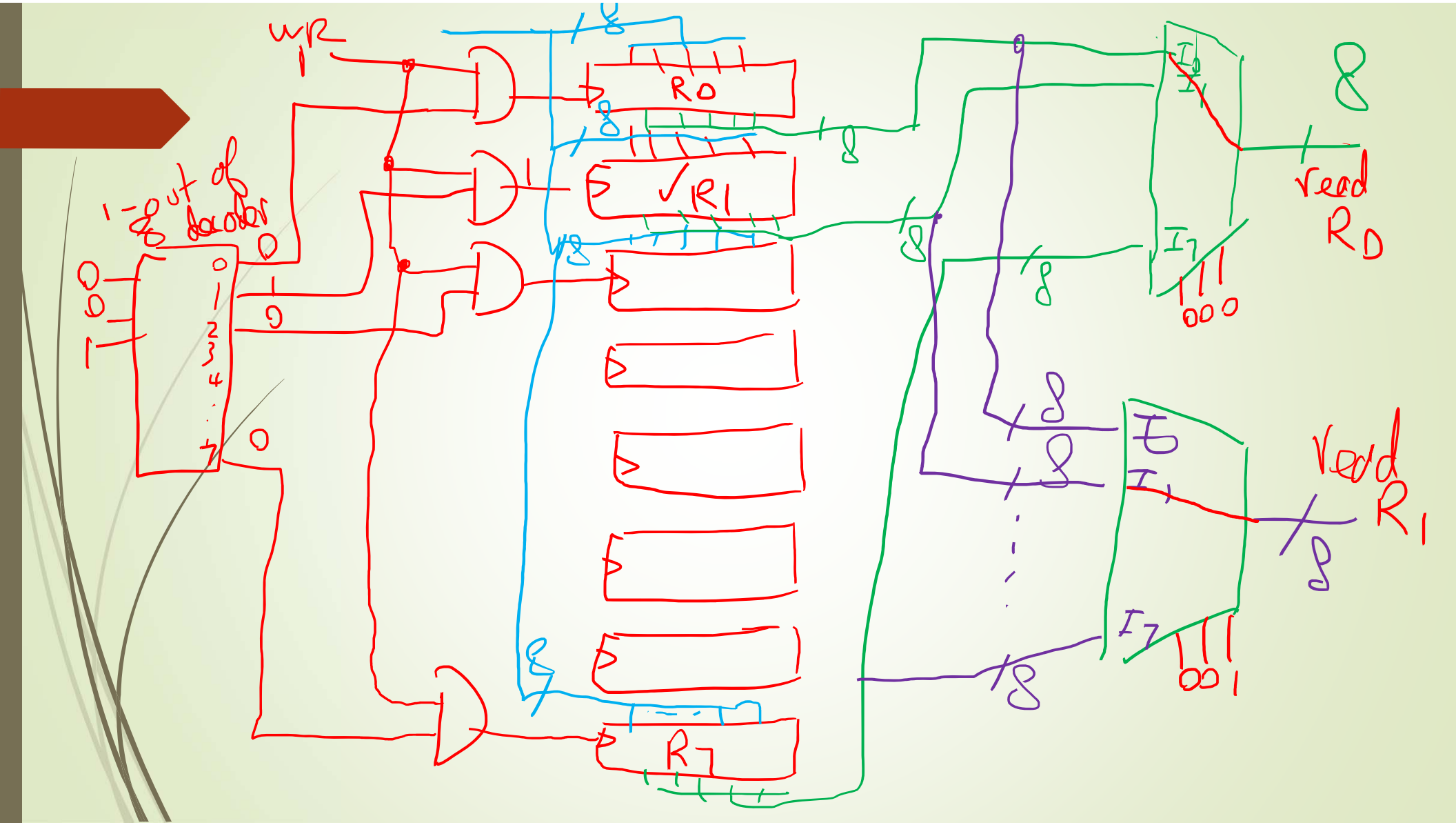


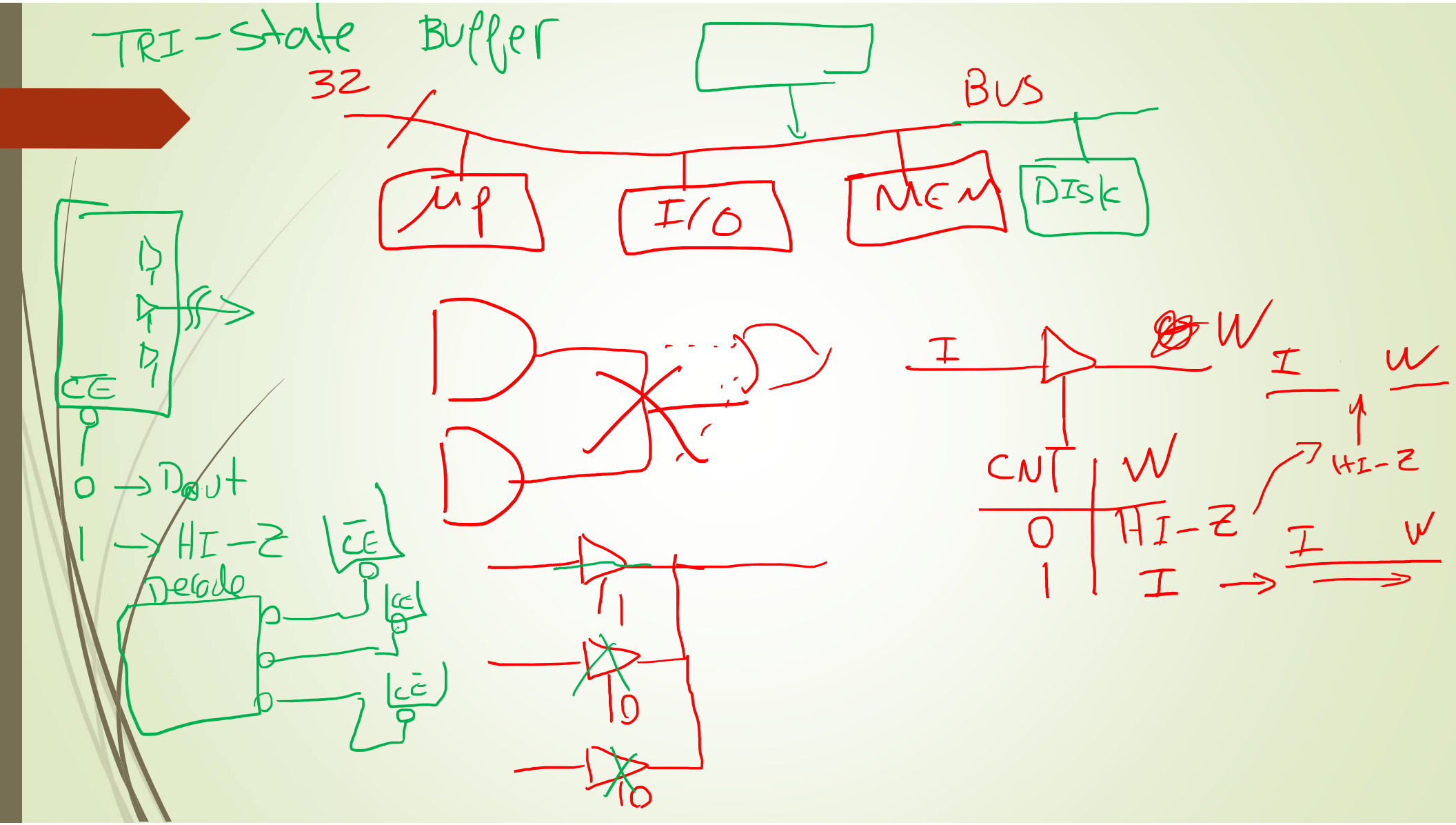
17.

a. Using D flip-flop, design an 8-bit register.

b. Using part a as well as other devices such as multiplexers, decoders, and gates, design a register file with 16 8-bit registers such that it can allow reading of any two registers and writing of any one.




WR
R0
R1
R7
1-8 out of decoder
0
0
1
0
1
2
3
4
7
0
I0
I1
I7
000
Read R0
001
Read R1


TRI-state Buffer
32
BUS
μp
I/O
MEM
Disk
CE
0 → Dout
1 → HI-Z
Decode
CE
CE
CE
I
W
I
W
CNT
W
0
HI-Z
1
I
HI-Z
I
W